

REMARKS

Claims 1-3, 6-14, and 17-19 are pending in the present application. Claims 4-5, 15-16, and 20-43 were previously cancelled. Claim 13 has been amended herein. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

Claims 1-3, 6, 7, 9-14, 17 and 18 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Matsumoto, et al. (U.S. Patent No. 6,455,894 B1, hereinafter "Matsumoto") in view of Paton, et al. (U.S. Patent Application Publication No. 2002/0111021 A1, hereinafter "Paton"). Applicants respectfully traverse these rejections.

Claim 1 recites at least one of the distinguishing features of the present invention, namely, "a first dummy silicide structure . . . formed completely over an isolation region, the isolation region comprising a dielectric material in a recess in the semiconductor substrate." The Office Action asserts that the substrate recited in Applicants' claim 1 is disclosed by the combination of the silicon layer 3, the buried insulating film 2, and silicide regions 10c and 10d of Matsumoto, and that the isolation region recited in Applicants' claim 1 is disclosed by the dummy gate insulating film 4c of Matsumoto. This is simply incorrect.

Applicants' claim 1 explicitly recites that the isolation region is formed *in a recess* in the semiconductor substrate. In the previous response dated July 14, 2008, Applicants noted that the silicide regions 10c and 10d could not be considered part of the substrate, and provided as an example information regarding the formation of the silicide regions 10c and 10d. In response, the Office Action stated that "the only requirement

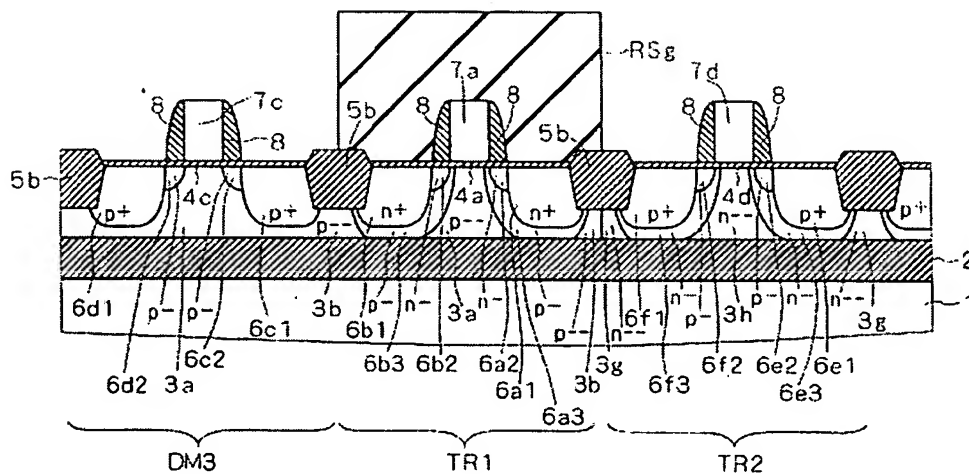
that a 'substrate' requires is that it support a layer thereupon." Office Action, page 7.

Applicants submit that even using this definition asserted by the Office Action the silicide regions 10c and 10d cannot be considered the substrate as explained below.

According to the Office Action, the silicide regions 10c and 10d may be considered part of the substrate with respect to the dummy gate insulating film 4c *only if the silicide regions 10c and 10d support the dummy gate insulating film 4c*. As clearly shown in Matsumoto, the silicide regions 10c and 10d never support the dummy gate insulating film 4c.

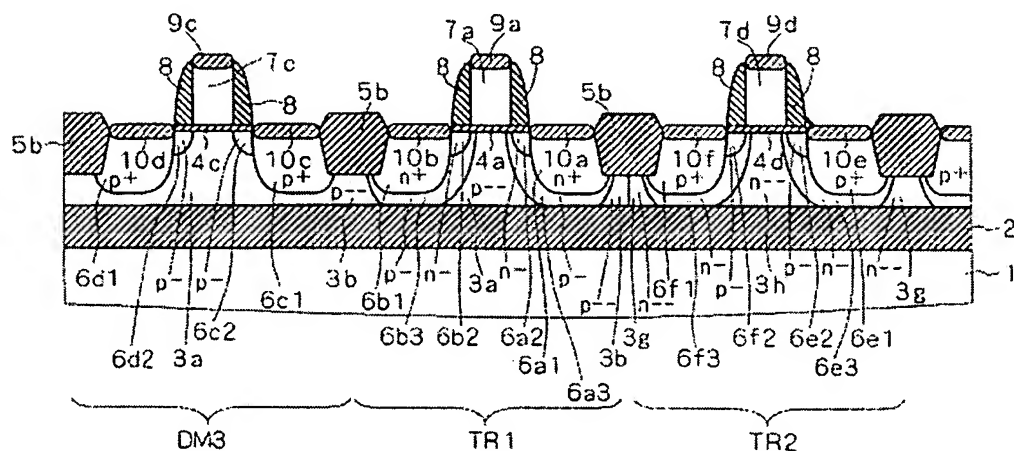
For example, beginning with Figure 36 of Matsumoto, a copy of which is provided below for reference, the dummy gate insulating film 4c is deposited over the silicon layer 3. Notably, at this stage it cannot be said that the silicide regions 10c and 10d *support* the dummy gate insulating film 4c, particularly since the silicide regions 10c and 10d have yet to be formed at this stage.

Figure 36 of Matsumoto



Continuing with Figure 37 of Matsumoto, a copy of which is provided below for reference, portions of the dummy gate insulating film 4c are removed and the silicide regions 10c and 10d are formed on opposing sides of the remaining portions of the dummy gate insulating film 4c. It should be noted that the silicide regions 10c and 10d are formed on opposing sides of the dummy gate insulating film 4c and does not support the dummy gate insulating film 4c. As such, it is clear that the silicide regions 10c and 10d are not part of the substrate according to the Examiner's own definition of "substrate."

Figure 37 of Matsumoto



The Office Action considered explanations similar to this in previous responses as invoking the Product-by-Process doctrine. Applicants disagree. The above discussion regarding the formation of the device referenced in Matsumoto illustrates that the silicide regions 10c and 10d are not part of the substrate. In particular, above discussion clearly illustrates that the silicide regions 10c and 10d cannot be considered part of the substrate under the Examiner's own definition – the silicide regions 10c and 10d *never support* the

dummy gate insulating film 4c, nor is the dummy gate insulating film 4c *on* the silicide regions 10c and 10d.

Using the logic asserted in the Office Action, the contact plugs 12a and 12b may also be considered part of the substrate with respect to the dummy gate insulating film 4c. Both the contact plugs 12b/12f and the silicide regions 10c/10d are both formed in the final device, but after the dummy gate insulting film 4c. Clearly the contact plugs 12b/12f are not considered part of the substrate relative to the dummy gate insulating film 4c. What is different about the silicide regions 10c and 10d that allow the silicide regions 10c and 10d to be considered part of the substrate relative to the dummy gate insulating film 4, but the contact plugs 12b and 12f are not? Applicants submit that there is nothing different regarding these structures and that neither of these structures may be considered the substrate to the dummy gate insulating film 4c.

In summary, Applicants assert that the silicide regions 10c and 10d cannot be considered part of the substrate using the very same definition asserted by the Examiner, *i.e.*, “the only requirement that a ‘substrate’ requires is that it support a layer thereupon,” for at least two reasons: (1) the silicide regions 10c and 10d do not support the dummy gate insulating film 4c; and (2) the dummy gate insulating film 4c is not on the silicide regions 10c and 10d. Accordingly, by the Examiner’s own admission, the silicide regions 10c and 10d cannot be the substrate relative to the dummy gate insulating film 4c.

In view of the above remarks, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Claim 13 has been amended to recite at least one of the distinguishing features of the present invention, namely, “the dielectric layer being a separate layer from the isolation region and being interposed between the silicide layer and the isolation region.” The cited references fail to disclose this limitation, and accordingly, Applicants respectfully request that the rejection of claim 13 be withdrawn.

Claims 2, 3, and 6-12 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 14 and 17-19 depend from claim 13 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 1, 8, 13, and 19 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Matsumoto in view of Nakamura (U.S. Patent No. 5,739,574, hereinafter “Nakamura”). Applicants respectfully traverse these rejections.

Applicants reiterate that the rejections of, apparently, claims 1, 8, 13, and 19 are confusing. For example, the Office Action merely asserted in paragraph 2 that claim 1 was obvious over Matsumoto in view of Nakamura, but failed to provide any support or motivation. The Office Action’s rejection of claim 13 appears to be incomplete as well.

Nevertheless, Applicants respectfully assert that claims 1 and 13 are patentable for at least similar reasons as those discussed above. Accordingly, Applicants respectfully request that these rejections of claims 1 and 13 be withdrawn.

Claims 8 and 19 depend from and further limit claims 1 and 13, respectively. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

In view of the above, Applicants respectfully submit that this response complies with 37 C.F.R. § 1.116. Applicants further submit that the claims are in condition for allowance. No new matter has been added by this amendment. If the Examiner should have any questions, please contact Applicants' attorney at the number listed below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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